Customer No.: 31561
Application No.: 10/707,665
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AMENDMENTS

In The Claims

1. (original) A layout of nonvolatile memory, comprising:

a word line;

a bit line;

a plurality of metal-oxide semiconductor (MOS) transistor memory cells, each having a gate electrode, a first doped electrode, and a second doped electrode, wherein each of the first doped electrode is coupled to the bit line, and each of the gate electrode is coupled to a corresponding one of the word line; and

a shared coupled capacitor structure, coupled between the transistor memory cells of the adjacent bit line from the second doped electrodes,

wherein the shared coupled capacitor structure comprises at least two floating-gate MOS capacitors, wherein each of the floating-gate MOS capacitors comprises:

a floating-gate transistor having a floating gate, a first source/drain (S/D) region and a second S/D region; and

a MOS capacitor, coupled to the floating gate,

wherein the first S/D region is coupled to the second doped electrode of the corresponding one of the transistor memory cells, and the second S/D region is shared with an adjacent one of the floating-gate transistor.

2. (original) The layout of nonvolatile memory of claim 1, wherein two adjacent bit lines are grouped in a memory group, wherein all of the transistor memory cells between two adjacent

bit lines share the same shared coupled capacitor structure

3. (original) The layout of nonvolatile memory of claim 2, wherein all of the MOS capacitors are positioned one after one in series.

4. (original) The layout of nonvolatile memory of claim 1, wherein the second S/D region is coupled to a first voltage and a substrate end of the MOS capacitor is coupled to a second voltage.

5. (original) The layout of nonvolatile memory of claim 1, wherein each of the MOS capacitors comprises two N-type MOS capacitors and one P-type MOS capacitor between the two N-type MOS capacitors in abutting contact.

6. (currently amended) A nonvolatile memory cell, comprising:

a metal-oxide semiconductor (MOS) transistor, having a first doped electrode coupled to a bit line, a gate electrode coupled to a word line, and a second doped electrode;

a floating-gate MOS transistor, having a first source/drain (S/D) region coupled to the second doped electrode, a second S/D region coupled to a first voltage terminal, and a floating gate; and

a MOS capacitor, having a gate-capacitor electrode coupled to the floating gate of the floating-gate MOS transistor, and a substrate-capacitor electrode coupled to a second voltage terminal,

wherein when a read process is operated, the bit line is applied with an intermediate voltage to select the memory cell, the first voltage terminal is applied with a ground voltage, the second voltage terminal are applied with a first voltage, and the word line is applied with a second

voltage.

7. (original) The nonvolatile memory cell of claim 6, wherein when a programming process is operated, the bit line is applied with a ground voltage to select the memory cell, the first voltage terminal and the second voltage terminal are applied with a first voltage, and the word line is applied with a second voltage, so that hot electrons are injected into the floating gate of the floating-gate MOS transistor.

8. (original) The nonvolatile memory cell of claim 7, wherein the word line and the bit line of a non-selected memory cell are respectively applied with the ground voltage and a system voltage source.

9. **(cancelled)**

10. (currently amended) The nonvolatile memory cell of claim [[9]]6, wherein the word line and the bit line of a non-selected memory cell are both applied with the ground voltage.

11. (Currently amended) A nonvolatile memory cell, comprising:

a metal-oxide semiconductor (MOS) transistor, having a first doped electrode coupled to a bit line, a gate electrode coupled to a word line, and a second doped electrode;

a floating-gate MOS transistor, having a first source/drain (S/D) region coupled to the second doped electrode, a second S/D region coupled to a first voltage terminal, and a floating gate; and

a MOS capacitor, having a gate-capacitor electrode coupled to the floating gate of the floating-gate MOS transistor, and a substrate-capacitor electrode coupled to a second voltage terminal, ~~The nonvolatile memory cell of claim 6,~~ wherein when an erasing process is operated, the bit line and the word line are set to be floating or applied with a ground voltage, the first voltage terminal is applied with an erasing voltage, and the second voltage terminal is applied with the ground voltage.

12. (original) The nonvolatile memory cell of claim 11, wherein the word line and the bit line of a non-selected memory cell are both set to be floating or applied with the ground voltage.

13 – 17. (canceled)